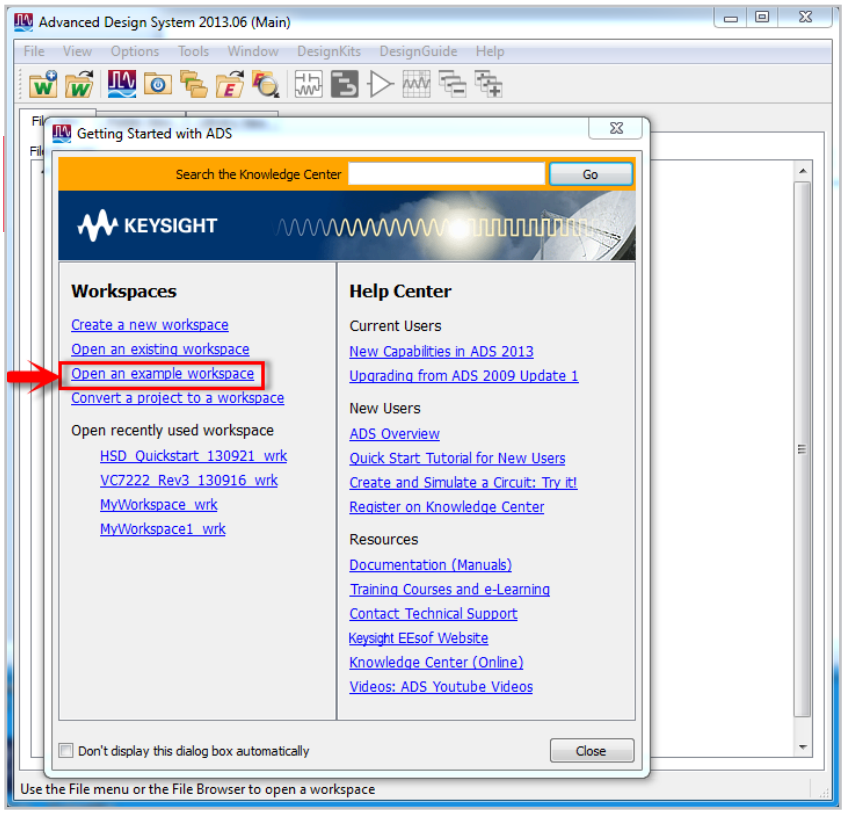
Quick Start for Signal Integrity Design Using Keysight Advanced Design System (ADS)

A part of the Keysight EEsof EDA High Speed Digital Design Workflow

Technical Overview



KEYSIGHT TECHNOLOGIES

Test Drive Keysight ADS Today!

– Are you a signal integrity engineer?

– Heard about ADS but haven't used it yet?

– Want a quick way to try it out for yourself?

Let's Get Started!

First, request an evaluation license at this link:
http://www.keysight.com/find/signal-integrity

– Click on the "Evaluate ADS" blue button:

http://www.keysight.com/find/eesof-ads-evaluation

– Send in the completed form.

– Download the installation executable file for your operating system from:
http://www.keysight.com/find/eesof-ads-latest-downloads

– Save the file to a new folder, for example C:\ads_install\.

– Inside that folder double click on the downloaded executable file, for example "ads2013_06_shp_windows.exe", and follow the installation instructions.

TIP:
The HOME directory sets the location of the hpeesof folder that is used to store all of the local user's customization of ADS. A different HOME directory should be used for each different release version of ADS that is installed.

Below, we will assume Windows and a default user workspace folder C:\ADS2013\, also known as your ADS "HOME" directory.

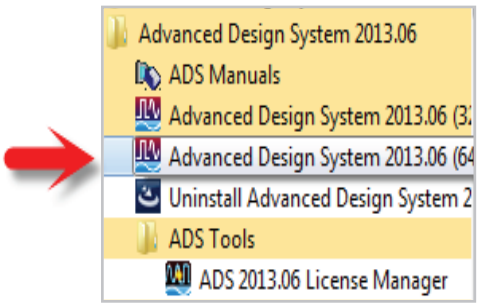
When you receive your license file (license.lic):

– Save a copy to the HOME directory C:\ADS2013\licenses\

– Double click on the ADS Desktop Icon, or from the Windows© Start menu, start ADS.

Desktop icon

Windows start menu

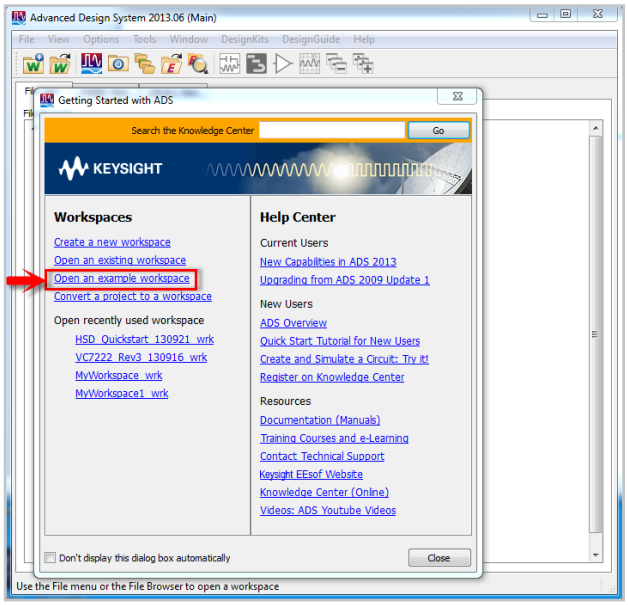


– When ADS opens, it will ask for the location of the license file. Add the license file by browsing to its location C:\ADS2013\licenses\license.lic.

A First Look at ADS Using an Example Project

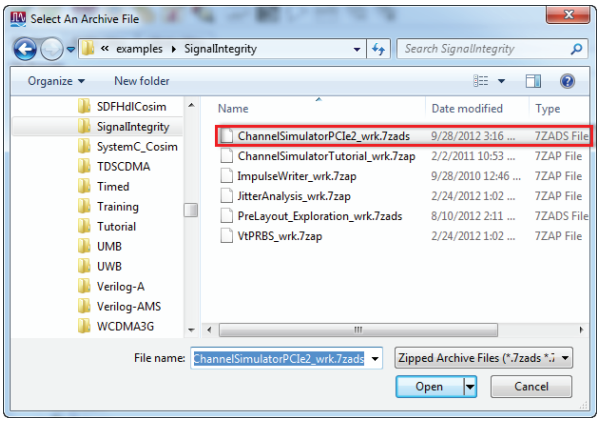
After the splash screen, the Main ADS window appears with the 'Getting Started with ADS' window over it. This has several Help Center links on the right, but since you will be following this guide, skip those for now. Instead:

– Click the ***Open an example*** workspace link:

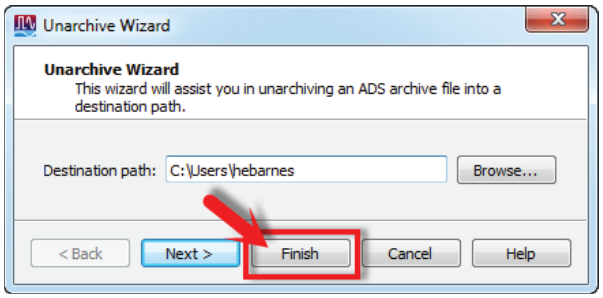


– Choose or double click on the Signal Integrity folder.

– Double click, or select and Open the ***ChannelSimulatorPCIe2_wrk.7zads*** archived workspace.



– The Unarchive Wizard opens. Use the default workspace settings by clicking on the ***Finish*** button.

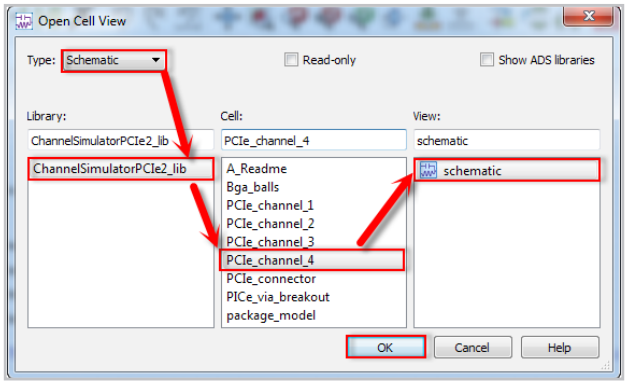


– The schematic window named A_Readme opens.

Simulate the Example Schematic

From the menu bar of this A_Readme schematic window, select ***File*** > ***Open***

– This opens the Open Cell View dialog box. ***Type*** is set to Schematic and the ***Library*** is the example workspace library ChannelSimulatorPCe2_lib. In the ***Cell*** column click on PCIe_channel_4 to select this ***Cell*** and then click ***OK*** to open this schematic ***View***.



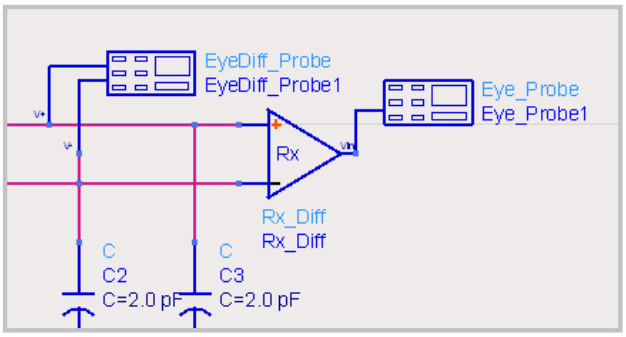
– ADS uses a powerful open access ***Library*** structure that organizes your designs into libraries that contain ***Cells*** (sub-folders) for organizing specific component ***Views*** (files) such as schematic, layout, and symbol.

– The schematic (a PCI Express design) opens.

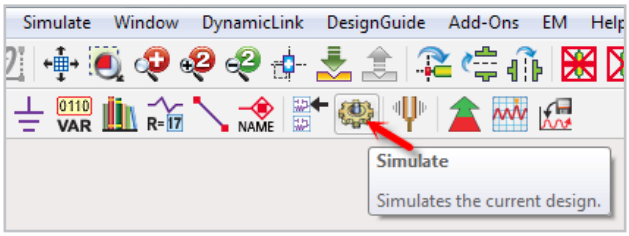
TIP:
The mouse scroll wheel can be used to zoom in and out on the schematic. Also, the ***View*** *menu and toolbar icons have additional navigation tools*

.

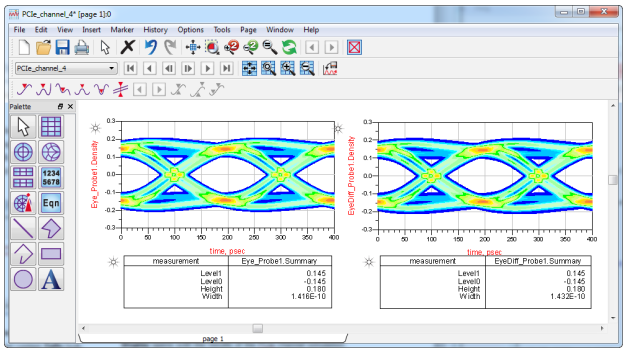
– Note that the components EyeDiff_Probe1 and Eye_Probe1 are collecting data before and after the receiver component, Rx_Diff.



– In the tool bar of this schematic window, click on the ***Simulate*** icon:



First the ***hpeesofsim*** status window opens with some warnings (ignore these for now), and then status messages about the simulation progress will follow. After a minute or so the ***PCIe_channel_4 Data Display*** opens with the results of the PCIe channel simulation.

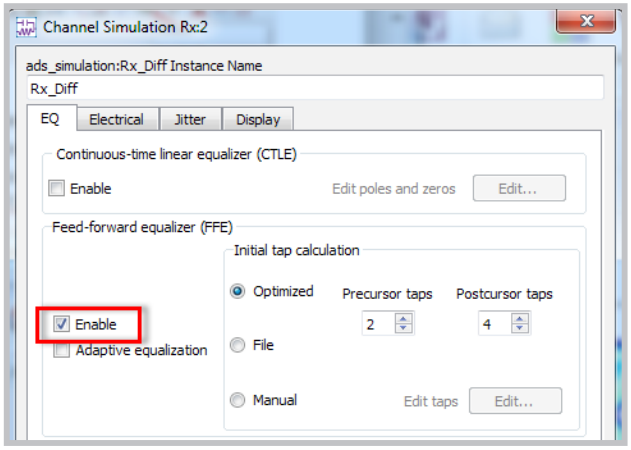


Modify the Schematic and Re-Simulate

The eye diagrams from ***EyeDiff_Probe1*** before and after Rx are nearly identical because the receiver equalization is turned off.

– Back in the schematic; double click on the ***Rx_Diff***  component to open its dialog box.

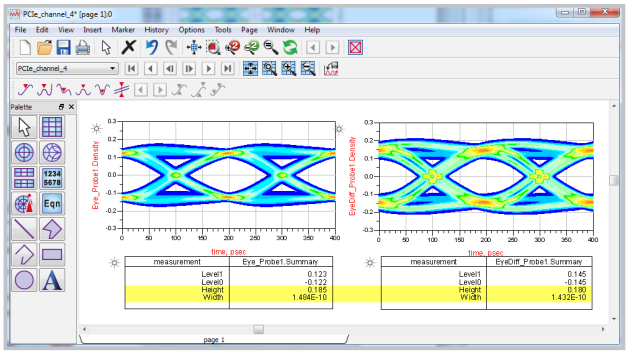
– Enable the ***Feed-Forward Equalizer (FFE)***



– Click ***OK*** to close the dialog box and save the changes.

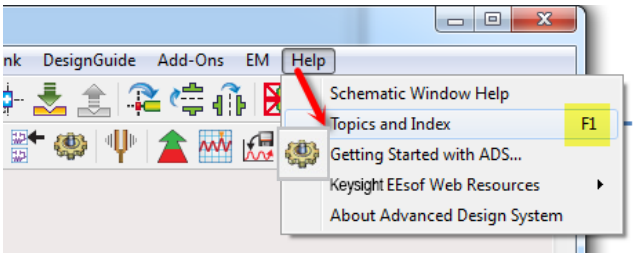
– Click the ***Simulate*** icon  .

– After completion, the data display window updates. Note the improvement in the post-receiver eye height and width.



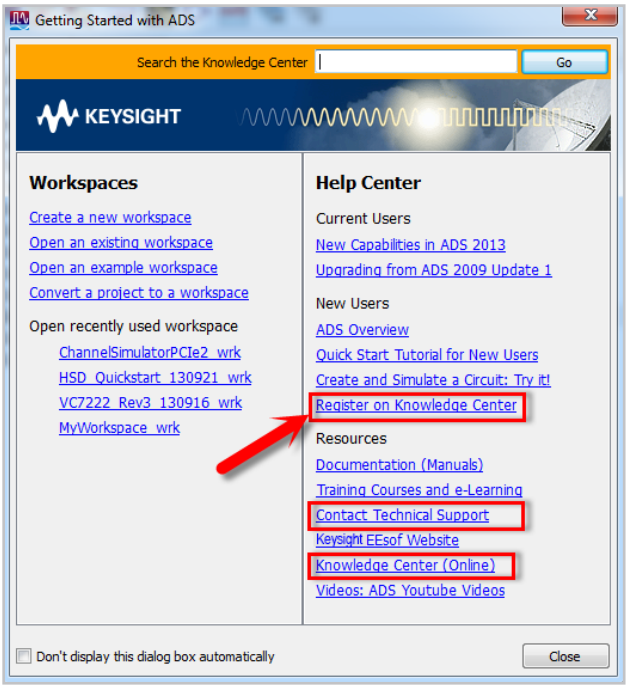
TIP:

*Help is just a click away. The **Help** > **Topics** and **Index** menu pick shows that there is also a one-click hot key for opening the built-in ADS documentation. Just press the **F1** function key at any time to open the documentation and use the **Search** tab to find specific topics.*



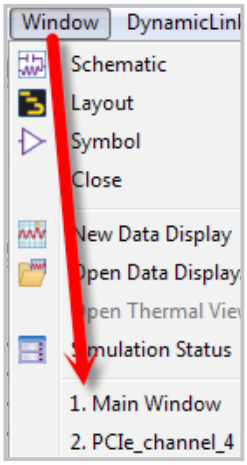
– The ***Help*** > ***Getting Started with ADS***... brings up the opening ADS splash screen with links to ***Technical Support*** and the on-line ***Knowledge Center*** with the latest in ADS documentation updates and application examples.

– Be sure to ***Register on Knowledge*** Center to gain full access to Keysight Technologies, Inc. world class technical support.

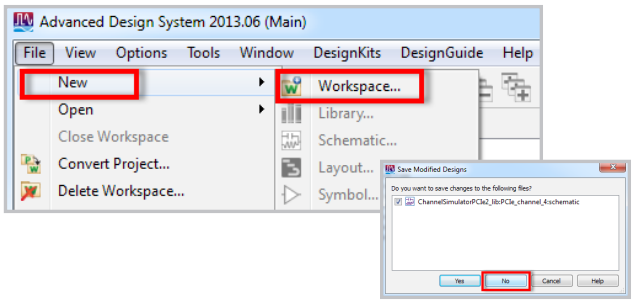


Start a New Project

– Switch to the ADS Main Window.
(Note that the ADS ***Window*** menu pick can be used to switch between open ADS windows)

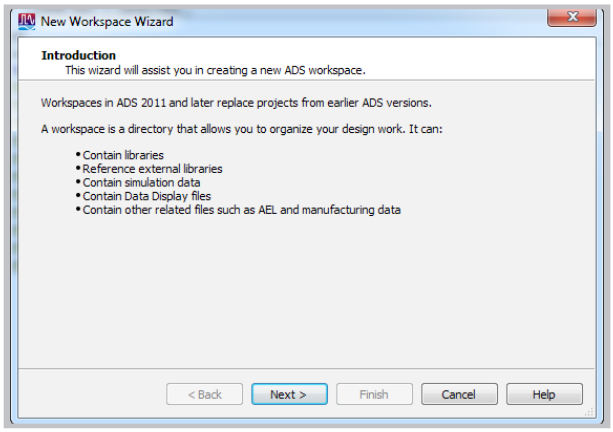


– Open a New Workspace by selecting ***File > New > Workspace***, and selecting No when asked if you want to save the changes you made to the PCIe Workspace example.

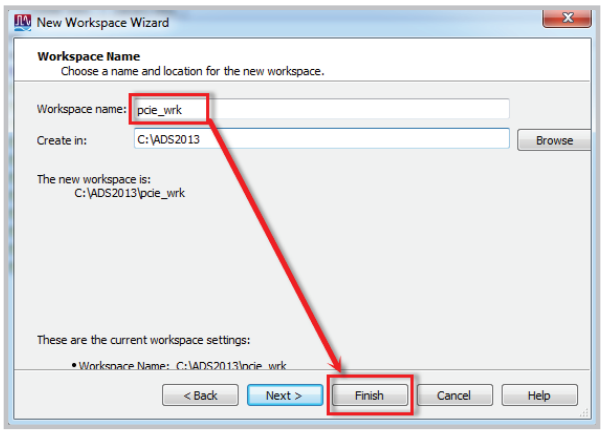


– ADS will close the existing workspace and then open the ***New Workspace Wizard***.

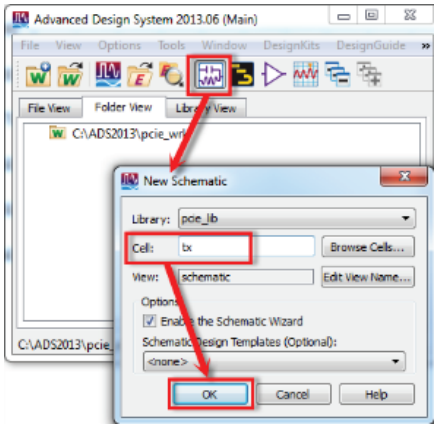
– Click ***Next*** to proceed to the Workspace Name page of the wizard.



– Enter ***pcie_wrk*** for the name of the new Workspace. Other options are available, but at this point select ***Finish*** to have ADS use the default library settings for the new workspace.

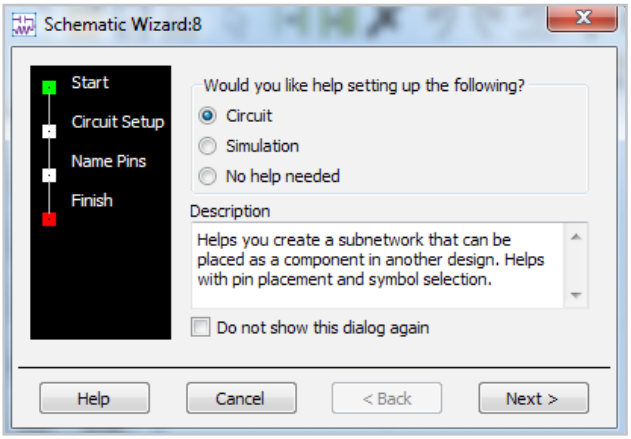


– Click on the Schematic Icon in the Toolbar to open a new schematic window. Enter ***tx*** for the library cell name that the new schematic will be ascociated with.

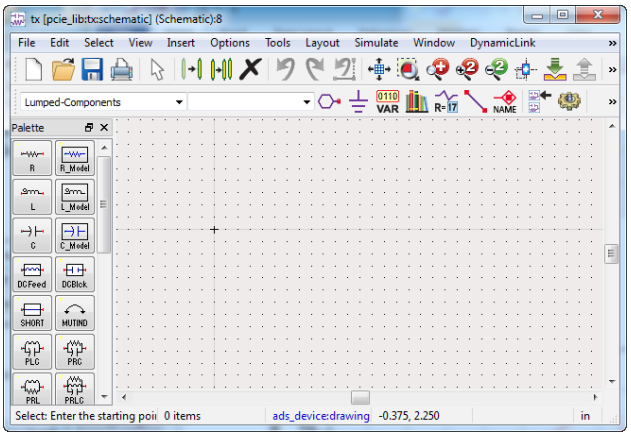


Creating the Design

Close the Schematic Wizard by clicking Cancel.



A blank schematic window appears:



From this point, there are only three steps between you and answers you need in ADS. We call them:

The A B C's of ADS

Schematic  Simulation  Display 

Summarized in 3 easy steps:

A) Place components, connection lines (called nodes), and a simulation controller onto the schematic. (The icon for schematic is  . Later, we will explore the option to associate layout artwork with a schematic. The layout icon is  .)

B) Create a dataset by clicking on the "run simulation" icon  .

C) Create a data display to view your results in. The icon for the data display is  .

That is it! That's all there is to it!

The ABC's will quickly become second nature to you. But for this first pass, let's walk through each one in detail by building a simple design to look at the eye diagram that we will be transmitting later on.

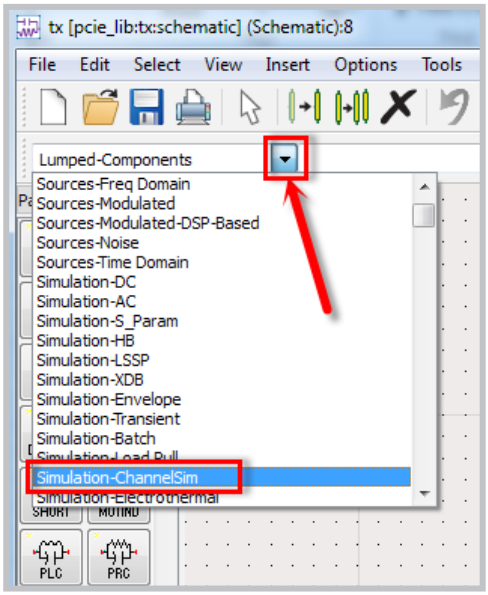
A. Place Components and Simulation Info on the Schematic

Mirroring the real world, there are thousands of components available in the ADS library  .

The palette on the left of the schematic is a tool to help organize them. By default, the Lumped-Components palette is displayed.

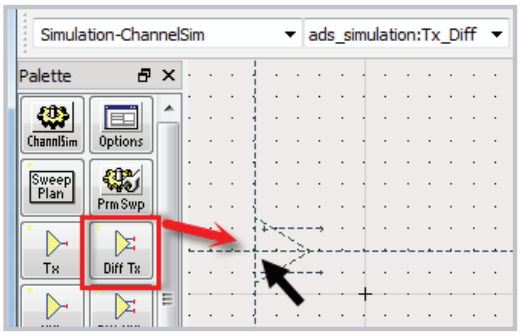
– Click on the down arrow  to show the list of available palettes.

– Scroll down and select the ***Simulation-ChanSim*** palette.



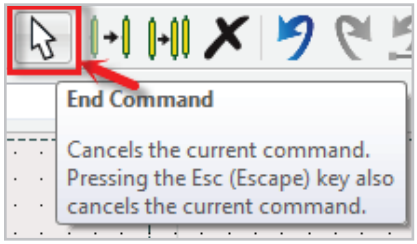
– Click on the ***Diff Tx*** (differential transmitter) icon  .

– The cursor becomes a crosshair with a ghostly image of the component:



– Click on the blank canvas to place the transmitter and create an instance of the component in your schematic.

– The ghost image remains, so cancel out of the command by pressing the Esc key or by clicking on the End Command icon  .



– Pick the ***Diff Term*** (differential termination) icon from the ***Simulation-ChanSim*** palette and place it to the right of the transmitter  .

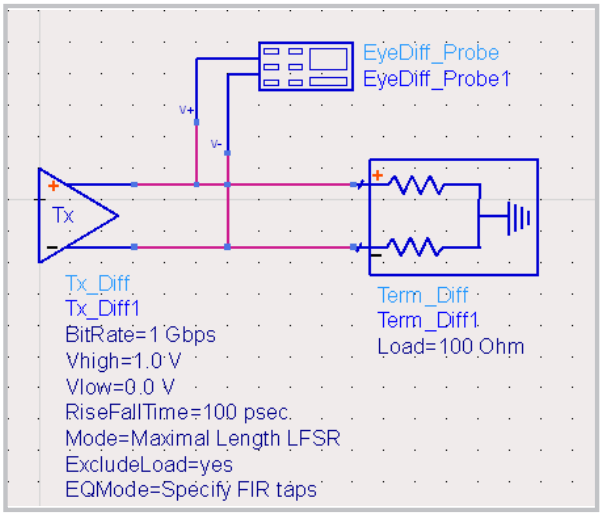
Some components are used so much they live not in a palette but on the toolbar, e.g. Wire and Ground.

– Pick the Wire icon  :

– Join the + and – nodes to + and -, respectively. The red dot turns blue to indicate connection has been made  .

A. Complete the Schematic

– Pick and place the ***EyeDiff PROBE***  (differential eye probe) from the ***Simulation-ChannelSim*** palette onto the schematic. The schematic should have three connected components.



TIP:

Any time you make a mistake, you can simply click on the undo button  *on the toolbar. If you change your mind, you can undo the undoing by clicking on the redo button*  .

You can set up the parameters of a given component instance directly on the schematic or via its dialog box. We will use the latter method for now.

– Double click on the ***Tx_Diff1*** instance  to open its dialog box.

On the ***PRBS*** tab set:

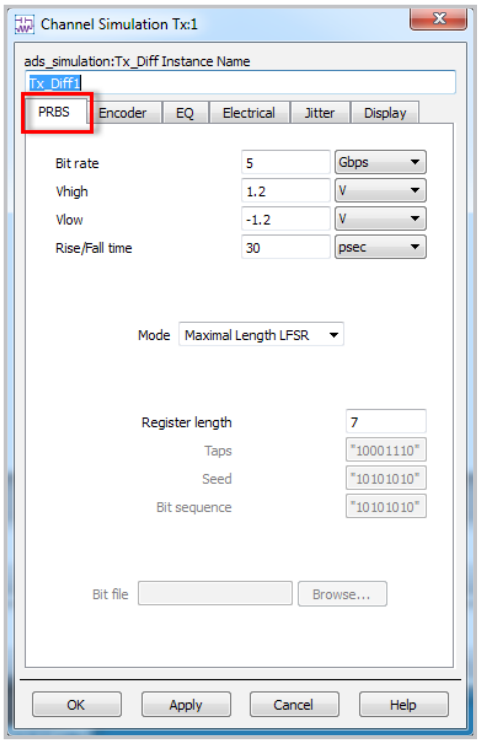
– Set Bit Rate = 5 Gbps

– Vhigh = 1.2V

– Vlow = -1.2V

– Rise/Fall Time = 30 ps

– Register Length = 7



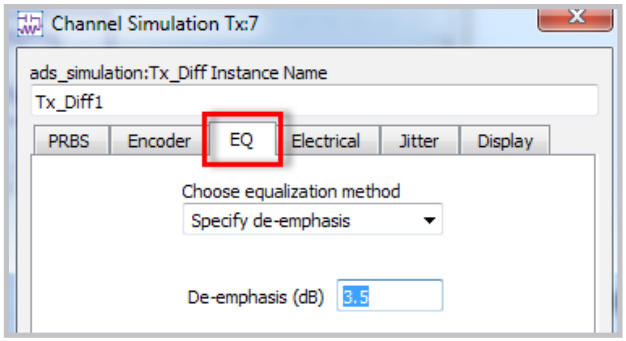
Click on the [***Help***] button at the bottom of the dialog box to bring up the documentation page for the Tx_Diff component.

The documentation pages contain a wealth of information about the parameters and algorithms used.

A: Set Component Parameters, (Continued)
B: Simulation Controller and Simulation
C: Data Display

– On the ***Encoder*** tab set the encoding to ***8B10B***.

– On the ***EQ tab***, set ***Choose equalization method*** to ***Specify de-emphasis*** and set De-emphasis as a positive quantity, ***3.5*** dB is a typical value.

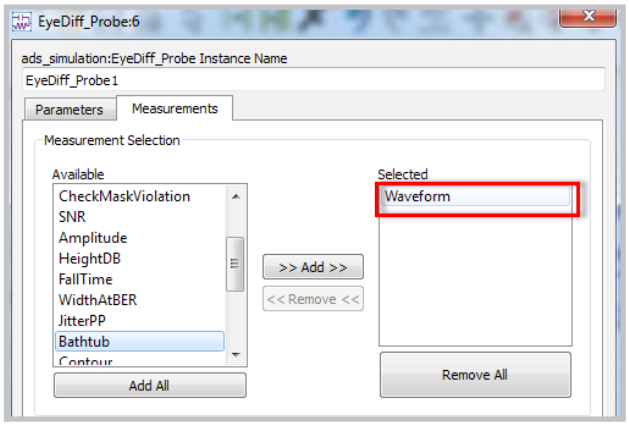


– Click ***OK*** to dismiss the ***Tx_Diff1*** dialog box.

– Double click on ***EyeDiff_Probe1***.

– In its dialog box, set the ***Data rate*** to 5 Gbps.

– Click on the ***Measurement*** tab, click on the [***Remove All***] button under the ***Selected*** list. Then select the ***Waveform*** in the ***Available*** list and use the [>>***Add***>>] button to move it to the ***Selected*** list.

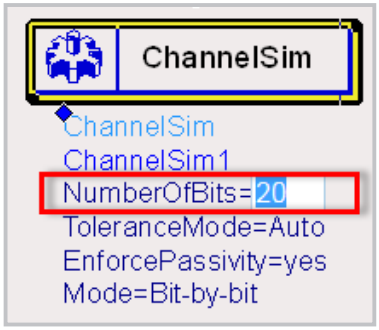


Step B: Simulation Controller and Simulation

– Click on the ***Channel Simulator*** icon  on the ***Simulation-ChannelSim*** Palette.

– Drop the controller onto the schematic, then hit ***Esc*** to ***End Command***.

– Edit ***NumberOfBits*** to ***20***, by directly clicking on the schematic, then click elsewhere or hit ***Esc*** to ***End Command***.

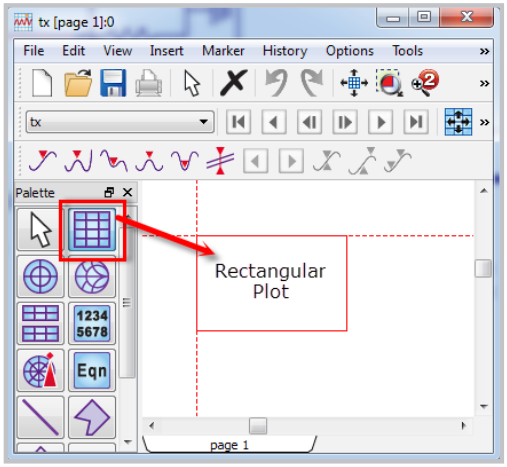


– On the schematic toolbar, click on ***Simulate***  .

Again the status window opens, the simulation runs in a few seconds, and then the data display window opens.

Step C: Data Display

– In the data display palette, click on the ***Rectangular Plot*** icon and place a blank plot onto the display by clicking and dragging the cursor to set the plot area.



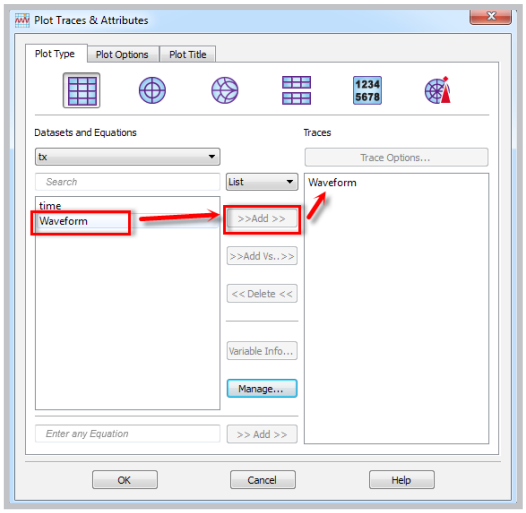
C: Data Display (continued)

When you drop a fresh plot onto the data display canvas, its dialog box opens automatically, with the default data set tx selected.

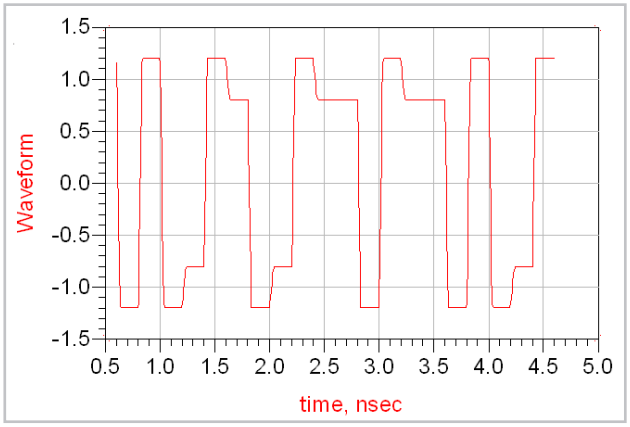
– Select ***Waveform***.

– Click the [>> ***Add*** >>] button.

– Click ***OK***.

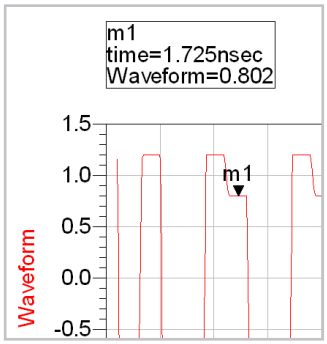


The plot appears. When a one follows a one or a zero follows a zero de-emphasis has been applied. Check the voltage.



– Click ***Insert a New Marker*** icon .

– Click on a one bit that follows another one bit:

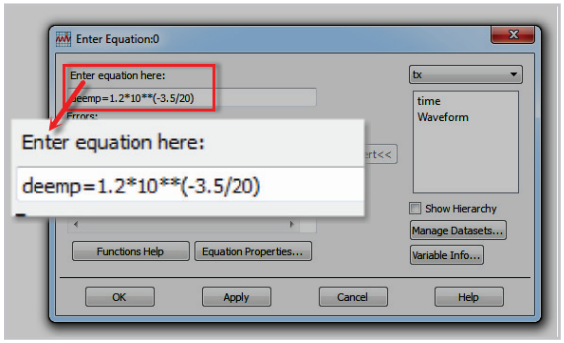


The de-emphasis is 0.802 V. Data display equations are handy for all sorts of things including calculation of check values.

– In the ***Data Display Palette***, select ***Eqn***. 

– Drop the equation onto the canvas.

– In its dialog box, enter the following equation:



– Click ***OK***.

– In the ***Data Display Palette***, select ***List*** 

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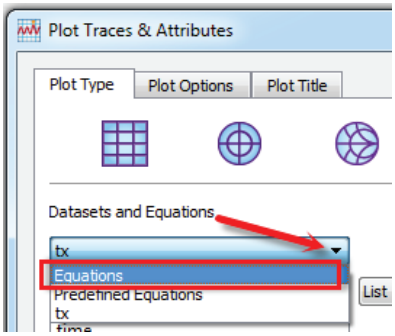
C: Data Display, DesignGuide Installation (continued)

– Instead of the default dataset, select ***Equations*** from the drop down list.



– Select your ***deemp*** result and click the [>> ***Add*** >>] button

– Click ***OK***. As expected, the value agrees:

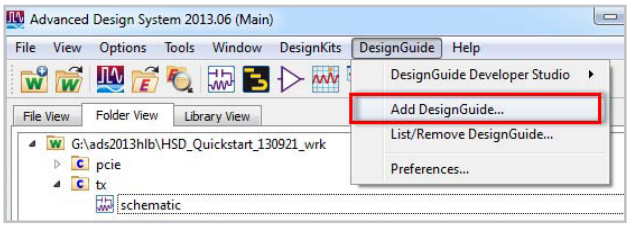
deemp
0.802

Congratulations!

You completed the first simple "A B C" project.

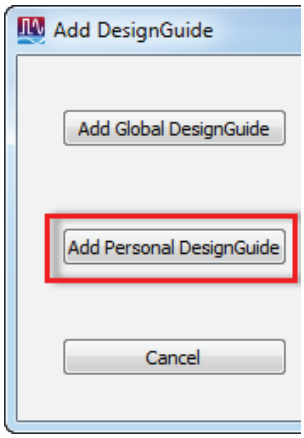
We'll pick up the pace now by using one of ADS's powerful features: DesignGuides. These are pre-built project templates and tools. In our case, we'll use one that jump starts our PCI Express project.

– Select ***DesignGuide > Add DesignGuide*** from the main ADS window.



– Click the [***Add Personal DesignGuide***] button.

– Navigate to and select the ***PCIE.DEB*** designguide located in the ADS installation directory.



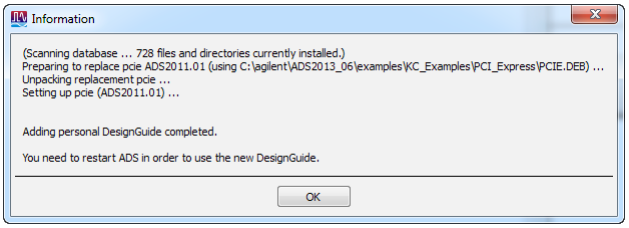
TIP:
The ADS installation directory path is stored as an ADS environment variable HPEESOF_DIR and its setting can be found by selecting the ***ADS Main menu Tools>Configuration Explorer*** *and scrolling down to the HPEESOF_DIR variable.*

– In this example HPEESOF_DIR=C:\keysight\ ADS2013_06 and the path to the PCIE.DEB designguide is:

C:\keysight\ADS2013_06\examples\KC_Examples\PCI_Express

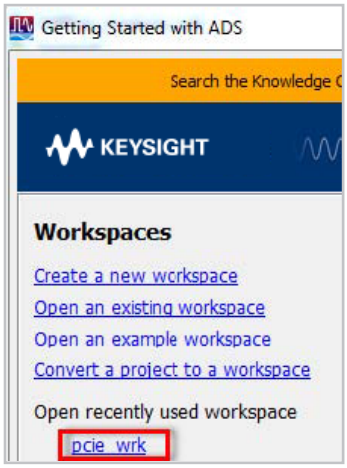
– Select the ***PCIE.DEB*** file and click the [***Open***] button.

– When the DesignGuide is finished installing an ***Information*** window will open. Click ***OK*** and then restart ADS by exiting the program and restarting to finish the installation of the designguide.



Determine Eye Diagram Performance for PCI Express Gen 2

When ADS opens use the ***Getting Started with ADS*** dialog window to select the previously created ***pcie_wrk*** workspace:



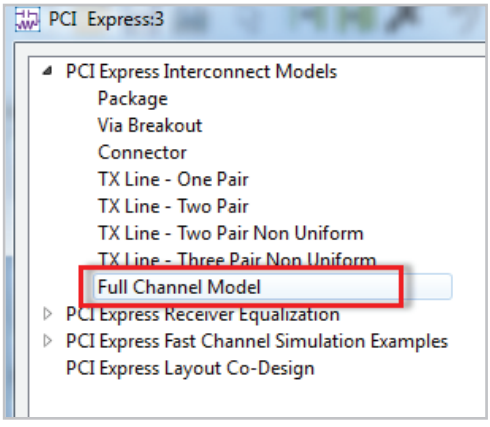
– Create a fresh schematic window, for example by clicking on the **schematic** icon in the ***ADS Main window***.

– Name the schematic cell ***pcie*** and click ***OK***.

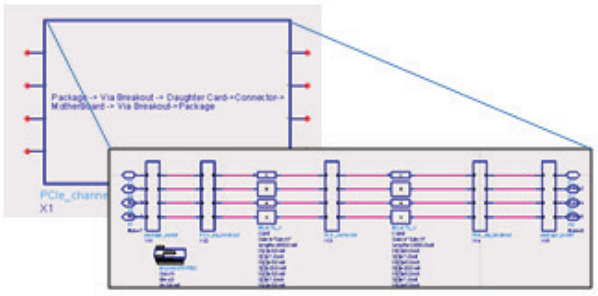
– ***Cancel*** the ***Schematic Wizard*** pop-up dialog window.

We'll add source/load impedance, transmitter and eye probe to the pre-built DesignGuide PCI Express channel, add crosstalk and simulate with and without equalization.

– On the pcie schematic place a ***PCI Express Channel model*** using the schematic's menu: ***DesignGuide ► PCI Express ► PCI Express Interconnect Models ► Full Channel Model***.

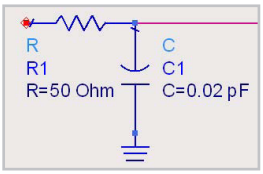


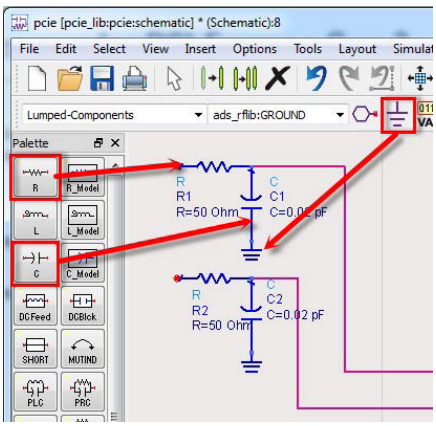
– Use the tool bar icon ***Push*** and ***Pop*** icons to explore the newly placed PCIe_channel_model component design hierarchy



Create the ***series R***, ***parallel C*** source termination using the ***ideal R*** and ***ideal C*** components in the ***Lumped-Components Palette*** and the ***Insert Ground*** icon in the ***Schematic Toolbar***.

R= 50 Ω, C=0.02 pF

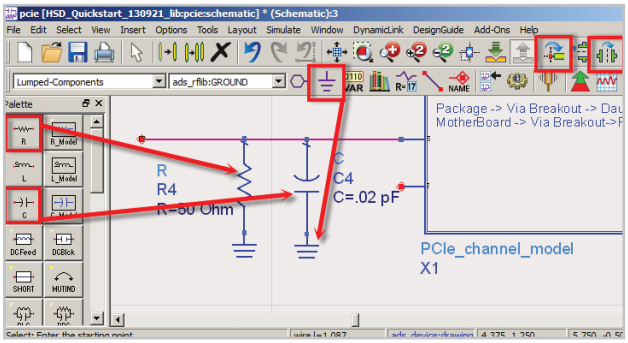




TIP:
Tool Bar Icon for Rotating a Selection.

Determine Eye Diagram Performance for PCI Express Gen 2 (continued)

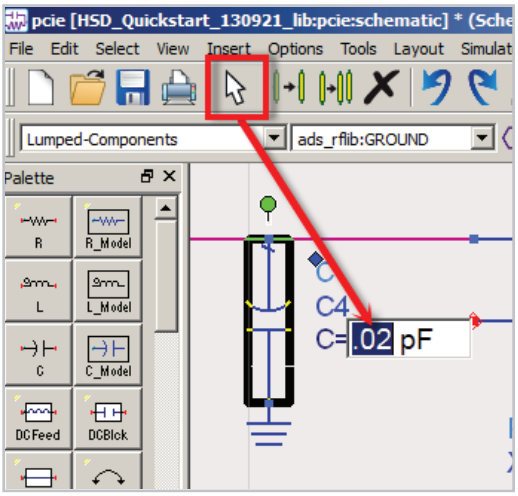
Create the ***parallel R, parallel* C** Load termination using the ***ideal R***  and ***ideal C***  components in the ***Lumped-Components Palette*** and the ***Insert Ground***  icon in the ***Schematic Toolbar.***



TIP:

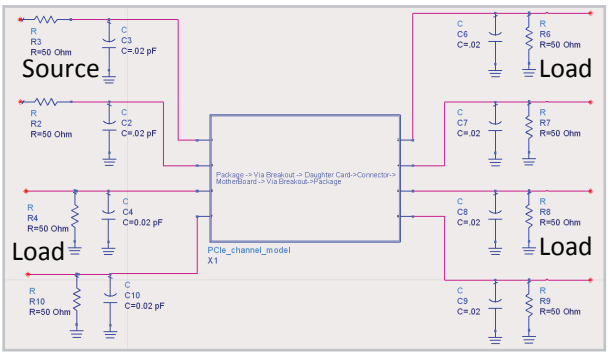
Use the Tool Bar ***rotate icon***  *and the* ***mirror icon***  *to create the parallel topology. Notice that typical keyboard combinations* ***CTRL-c*** *and* ***CTRL-v*** *work for copying and pasting items selected with the Tool Bar arrow icon*  *and clicking and dragging the selection box around items in the schematic.*

To change the capacitor value click on the value and then when the value is highlighted for editing type in the new value 0.02.



Add Source terminations to two of the ports and Load terminations to the remaining 6 ports.

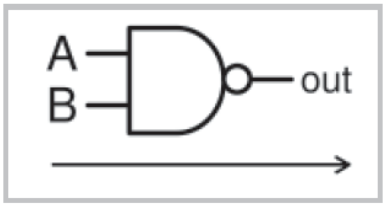
The component values are ***R= 50 Ω*** for the resistors, and ***C=0.02 pF*** for the capacitors.

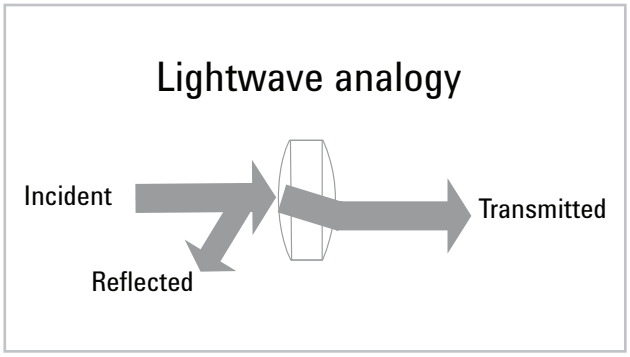


A Diversion into S-Parameters

If you pushed into the hierarchy, you'd have noticed some components were defined using S-parameters. So let's take a short break from the keyboard and first say why we use network parameters in general and S-parameters in particular, to characterize high frequency structures and components.

For low speed digital logic we only consider the forward propagation of signals, because, although reflections exists, they generally die down quickly if the interconnection flight time (propagation time) is short compared to the rise and fall times and the bit period. In fact, the incident signal or wave is partly transmitted and partly reflected:





Keysight Application Note AN 1287-1, "Understanding the Fundamental Principles of Vector Network Analysis"
http://literature.cdn.keysight.com/litweb/pdf/5965-7707E.pdf

So, instead of a single transfer function, it might seem we now need two parameters to characterize a 2-port component at each frequency. In fact, the situation is more complex. The output port is also being bombarded with waves reflected off of the component in front of it in the cascade. These reverse waves are also partly transmitted (backwards down the cascade) and partly reflected off of the output port (heading back up the cascade). So we actually need four numbers per frequency point. Each is a complex number, representing magnitude and phase of the respective wave, relative the incident wave.

For reasons given below, it is convenient to collect the four numbers together in a two-by-two matrix called network parameters. There are several formats each of which has their pros and cons. The most convenient format for measurement purposes is the S-parameter format, because you can measure S-parameters using standard load, source, and connector impedances such as 50 Ω. In contrast, direct measurement of, say, Z parameters requires opens and short loads and sources, which are difficult to make at high frequencies and can damage some components. Once you have the S-parameters measured, there are simple calculations to convert to other formats if needed.

For a 2-port network, the S-parameters are:

Description	Symbol
Desired transmission forwards of forward wave incident on the input port	S21
Unwanted reflection backwards of forward wave incident on the input port	S11
Unwanted transmission backwards of backward wave incident on the output port	S12
Unwanted reflection forwards of backward wave incident on the output port	S22

The beauty of network parameters is that you don't have to sum an infinite series of partly reflected and partly transmitted waves bouncing up and down the cascade. The trick is that you can easily calculate the network parameters of arbitrary cascade of two-port components using a simple matrix calculation. All the internal reflections inside the newly created "black box" can be ignored, and the cascade treated as a composite two-port network, characterized by only four parameters per frequency point.

Network parameters can be generalized to more than two-ports and more than simple cascade connection. Here we'll use a 4 X 4 matrix S-parameters to represent a four-port network: a pair of coupled transmission lines such as those used in a differential interconnect.

One of the things ADS does really well is convert frequency domain S-parameters into a time-domain model. Other tools often leave you with an incorrect non-causal or non-passive conversion.

For more information on S-parameters, please see Keysight Application Note AN 95-1, S-Parameter Techniques for Faster, More Accurate Network Design, by Richard W. Anderson:

– Scan of the classic 1968 article:

http://literature.cdn.keysight.com/litweb/pdf/5952-0918.pdf

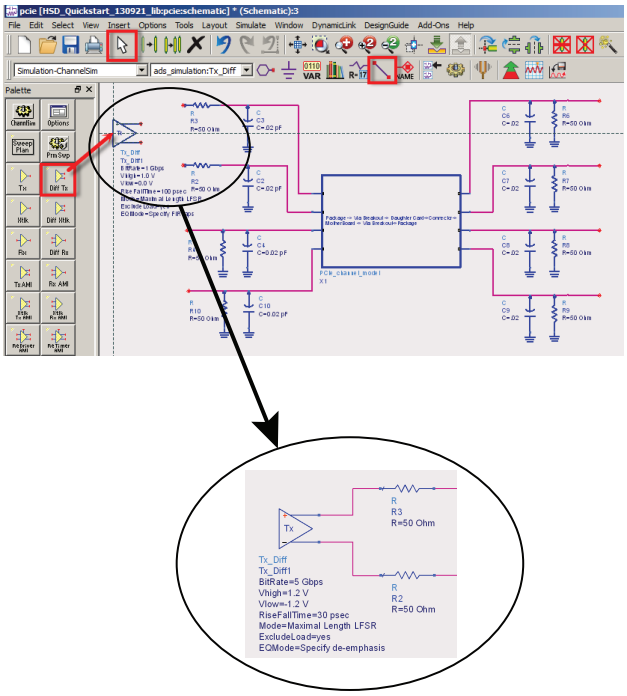
Now let's return to our PCI Express project...

Add the Transmitter

From the ***Simulation–ChannelSim palette***:

– Select ***Diff Tx***.

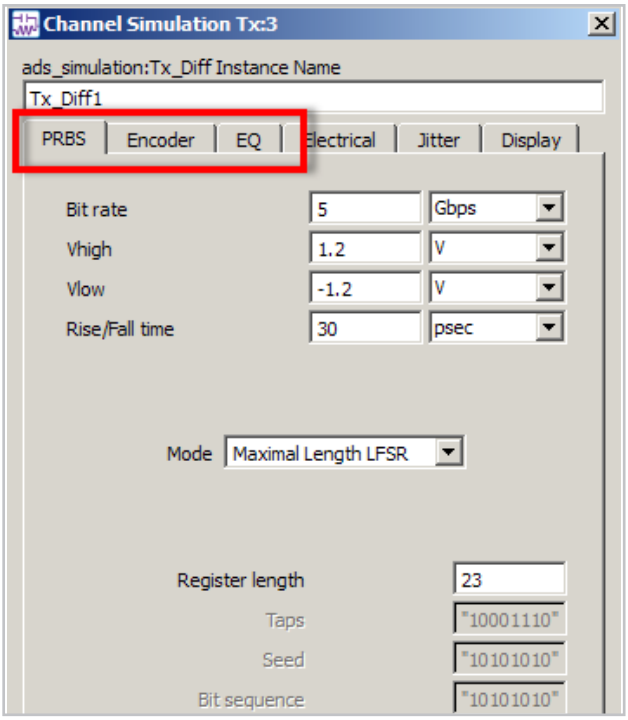
– Connect it to the input differential pins.



– Double click on ***Tx_Diff1*** instance.

– Go to the appropriate tabs to edit the following parameters:

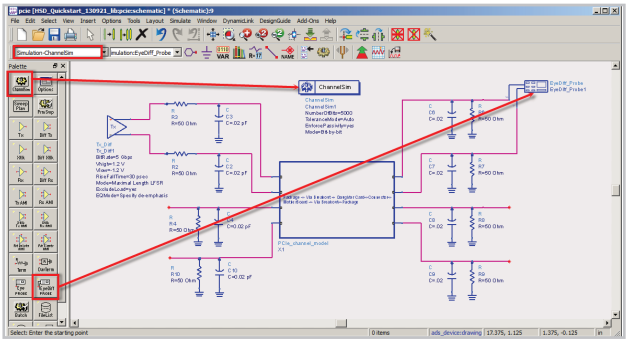
PRBS ▶ Bit rate	5 Gbps
PRBS ▶ Vhigh	1.2 V
PRBS ▶ Vlow	–1.2 V
PRBS ▶ Rise/Fall	30 ps
PRBS ▶ Register Length	23
Encoder ▶ 8B10B	Enable
EQ ▶ Specify de-emphasis	3.5 dB



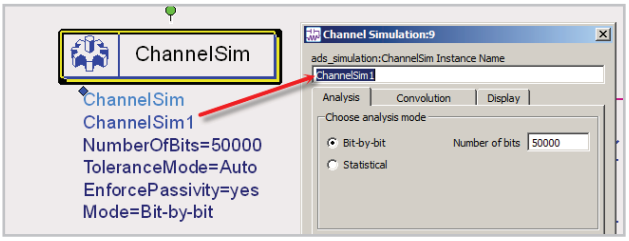
Add Eye Probe and Simulation Controller

– Select the ***EyeDiff_Probe*** from the same palette and connect it to the differential output pins.

– Place a ***Channel Simulation Controller*** (ChannelSim) on the schematic page.



– Set the ChannelSim1 parameter ***NumberOfBits*** to ***50000***.



– Click on the ***Simulate icon***  in the tool bar. A new data display window opens.

  – ***Save*** the ***data display*** as ***pcie.dds***.

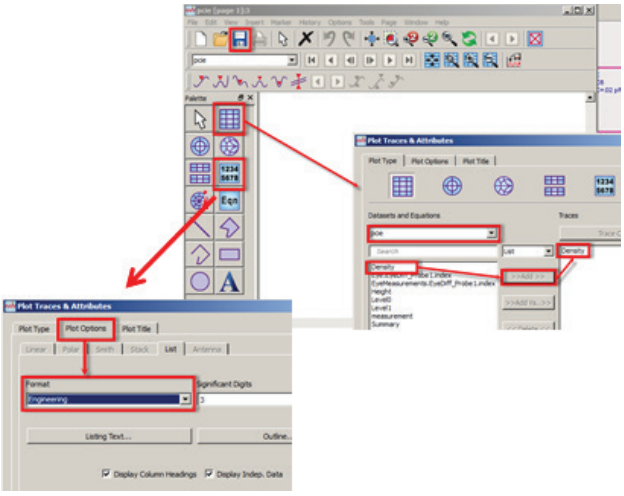
  – ***Place*** a rectangular plot and add the ***Density*** trace from the default pcie data set.

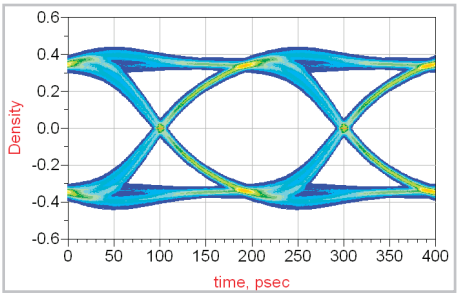
  – Place a ***List*** and add ***Summary*** measurements.

  – Select the ***Plot Options*** tab.

  – Select ***Format*** ▶ ***Engineering***.

  – Click ***OK***.



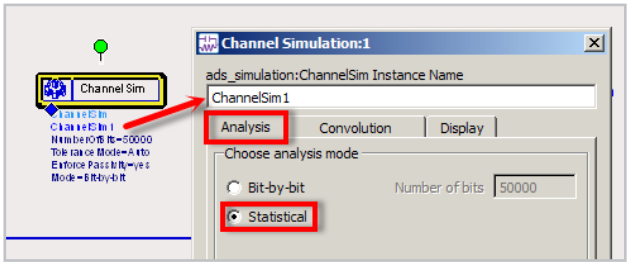


measurement	Summary
Level1	344.2 m
Level0	-344.2 m
Height	570.0 m
Width	184.0 p

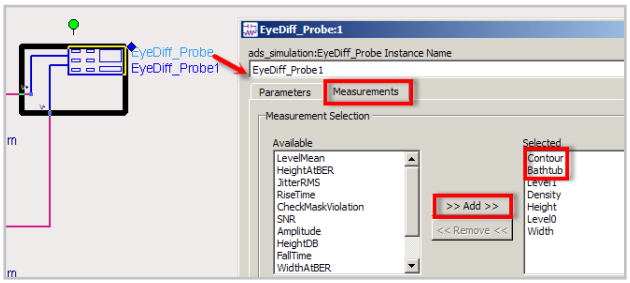
BER Contours Using Statistical Mode of Channel Simulator

– Go back to the ***pcie schematic.***

– Choose Statistical instead of Bit-by-bit mode by double clicking on the Channel Sim symbol and selecting ***Statistical radial button*** in the ***ChannelSim1*** ▶ ***Analysis*** tab.



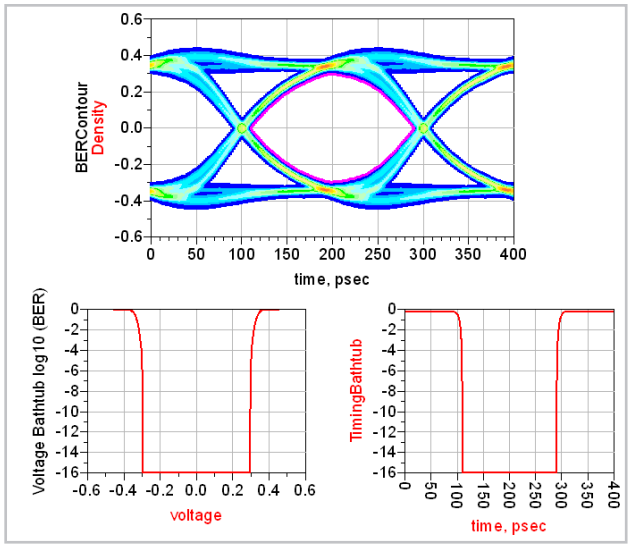
– Double click on the ***EyeDiff_Probe1*** symbol, select the ***Measurements*** tab and >> ***Add*** >> ***Bathtub and Contour*** to the selected list of measurements.



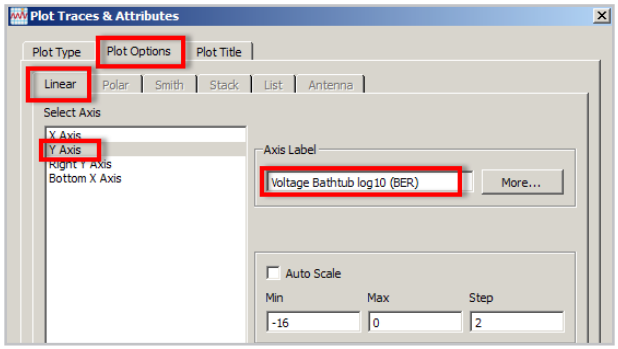
– Simulate 

– Double click on the data display density plot, then >> ***Add*** >> ***BER Contour***.

– Create new rectangular plots for ***VoltageBathtub*** and, separately ***TimingBathtub***.



– Double click on the ***Voltage Bathtub plot*** and customize the plot's Min, Max, Step, and axes Label by using the ***Plot Options*** tab.



Channel Simulator: Bit-by-Bit Mode

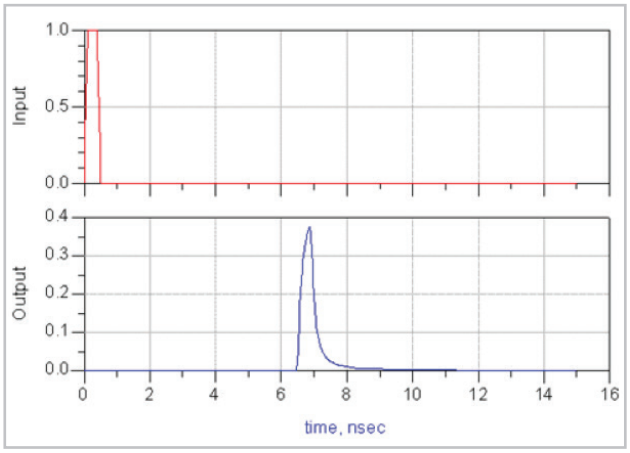
By now you might be asking, "What's the difference between traditional transient (SPICE-like) simulation and the two modes of Channel Simulator?"

Bit-by-bit mode works in two phases. First, we probe your schematic with a single step input. We use the transient simulator but we also automatically use convolution to deal with any components defined in the frequency domain and EM simulators to deal with distributed layout components. The computationally expensive transient simulation needs to run only for a short length of time, equal to the pulse response of the channel.

In phase two we use the step response from the above phase one as a linear time invariant model. We can then use computationally inexpensive superposition to calculate the output for millions of bits without having to call the transient, convolution, or EM simulators again.

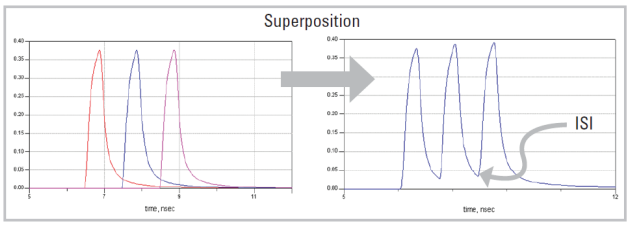
Phase 1:

SPICE-like transient response of single step – runs on existing schematic



Phase 2:

Million-bit-per-minute throughput using superposition

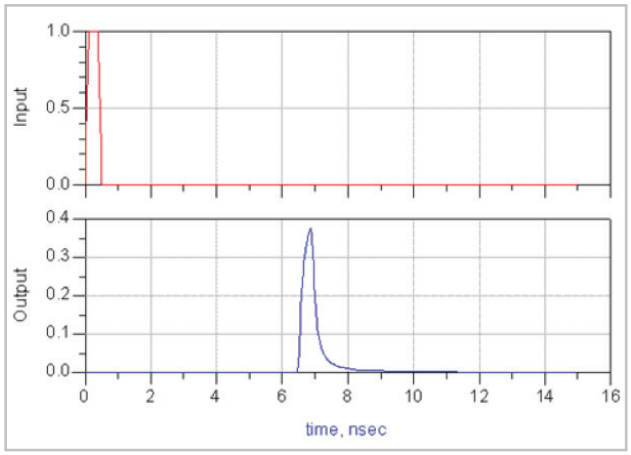


In statistical mode, again we have two phases. The first phase is the same as for bit-by-bit mode, but the second step is much quicker. There's no need for brute force superposition of each bit: just some mathematical calculations based on:

- ISI and crosstalk implied in the through and crosstalk pulse responses
- Jitter spec
- Equalizer spec
- Line coding

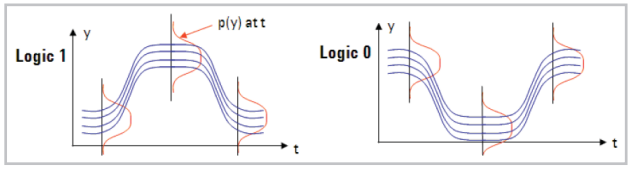
Phase 1:

SPICE-like transient response of single step – runs on existing schematic



Phase 2:

Million-bit-per-minute throughput using superposition



Comparison of Techniques

This table compares the three techniques:

	Transient (SPICE-like) simulator	Channel simulator bit-by-bit mode	Channel simulator statistical mode
Method	Modified nodal analysis of Kirchoff's current laws for every time step	Bit-by-bit superposition of step responses	Statistical calculations based on step response
Applicalibility	Any circuit	LTI channel; finite, user-specified bit pattern; adaptive or fixed eq. taps	LTI channel; strochastic props of infinite bit pattern; fixed eq. taps
BER floor in one minute simulation	~10^{-3}	~10^{-6}	~10^{-16}

Modeling Crosstalk, Comparing Two Simulation

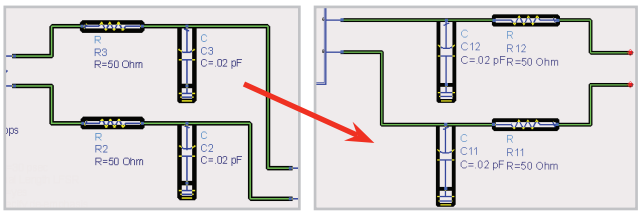
– ***Save*** the ***pcie schematic*** file. 

– Delete the load termination at the far end of the cross-talk channel (FEXT).

– Replace it by copying and pasting the source termina-tions that are on the input to the channel.

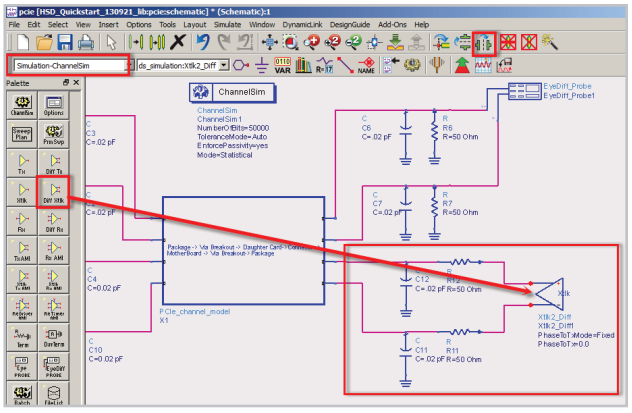
– > Select  > Copy Ctrl-c > Paste Ctrl-v > Mirror 

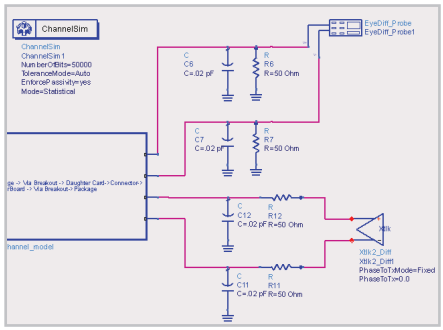
Then Click on the ***FEXT schematic*** location to place the source terminations.



– From the ***Channel Simulator Palette***, select the ***Diff Xtalk*** transmitter.

– Click Mirror About Y Axis  to flip the ghost image.



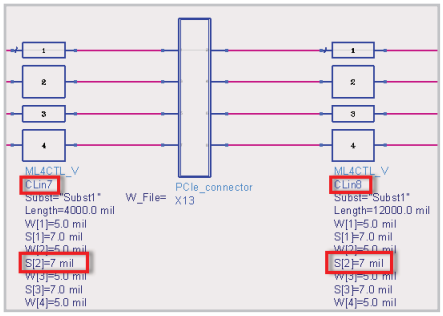


– Connect the crosstalk transmitter to the FEXT location with the new source termination.

Channel Simulator requires exactly one Tx component, but you can add as many Xtlk2_Diff aggressors as you need.

– Select the ***Random radio button*** of the ***Phase Relative to Tx*** setting of ***Xtlk2_Diff1*** ► ***PRBS***. We'll compare results with and without FEXT by saving the modified version with a different name.

– Push  into the ***Channel schematic*** symbol and change the spacing (S[2]) between the differential pairs from 20 mils to 7 mils to increase crosstalk on the ***CLin7*** and ***CLin8*** transmission line segments in the channel. ***Pop*** back to the ***Fext schematic***.



– From the schematic menu select ***File*** ► ***Save Design As***... and enter ***pcie_fext.***

Comparing Simulation With and Without Crosstalk

– ***Simulate*** 

A new, blank data display window opens, but we want to re-use the previous one, so:

– ***Close pcie_fext.dds***.

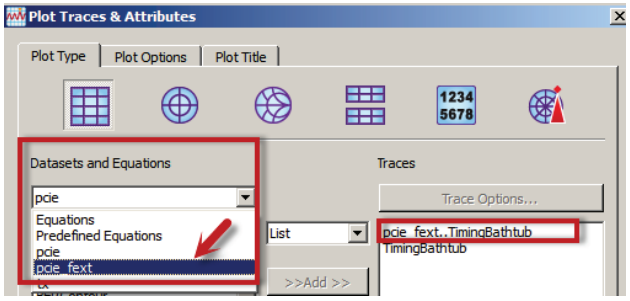
– Go to your previous ***pcie.dds data display*** window.

You can compare corresponding traces from two different datasets by using their full names. These have the format: ***dataset..trace*** (trace alone is just a shorthand for that item in the default dataset).

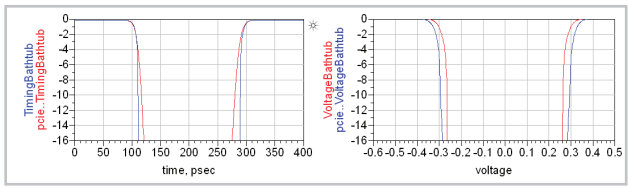
– Double click on the ***timing bathtub plot***.

– Select ***pcie_fext***, then add ***TimingBathtub***:

– Similarly, add a ***VoltageBathtub*** plot, and a ***List*** plot of ***Summary*** for ***pcie*** and ***pcie_fext***.



– Create a separate density and contour plot for the new data set.

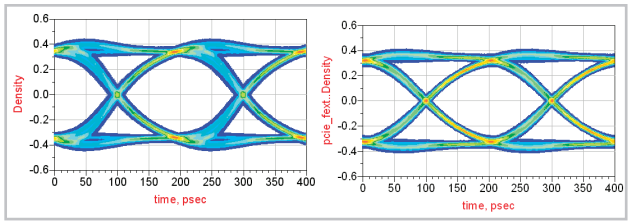


Let's see if we can push this design to a higher bit rate.

measurement	Summary	pcie_fext..Summary
Level1	344.7 m	316.6 m
Level0	-346.1 m	-320.4 m
Height	569.0 m	513.0 m
Width	178.0 p	181.0 p

– Overlaying two density and two contour traces on one plot is possible but messy, so:

– Create a separate density and contour plot for the new data set.



Let's see if we can push this design to a higher bit rate.

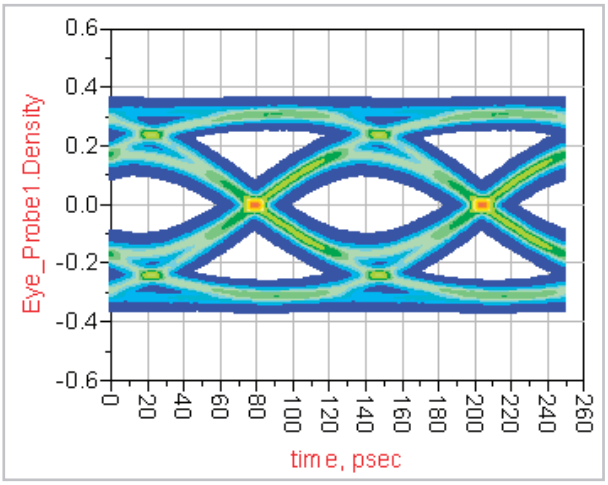
Explore the Design Space at 8 Gigabits per Second: Equalization

– Save  the 5 Gbps version of the schematic.

– Change the data rate of ***Tx_Diff1*** and ***EyeDiff_Probe1*** to 8 Gbps.

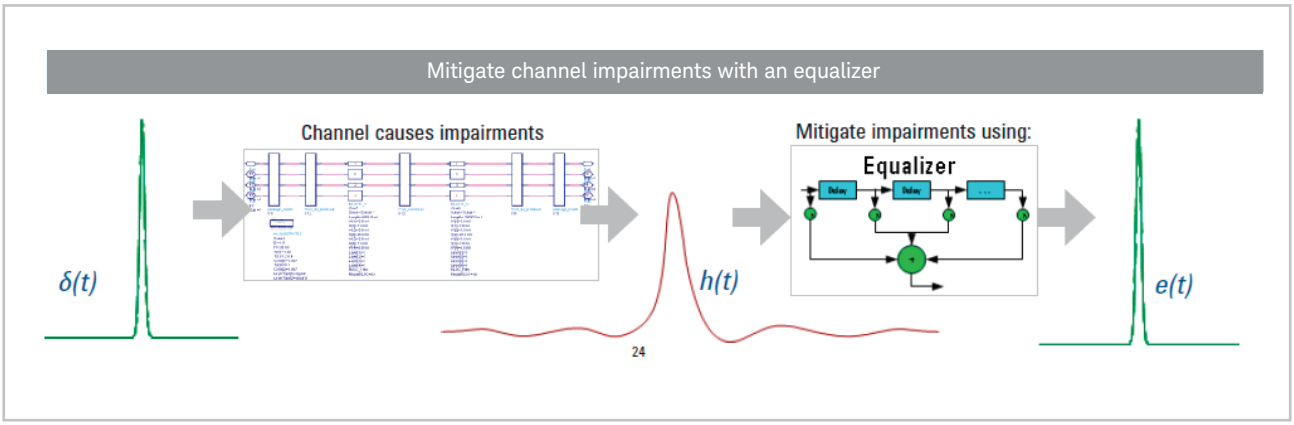
– ***File*** > ***Save Design As***... and enter ***pcie_fext_8***.

– Simulate  and compare with the eye diagram we did before.



How can we improve our margin? The channel impairs the signal by acting like a low pass filter, and introducing echo-like reflections. These smear out the impulse response.

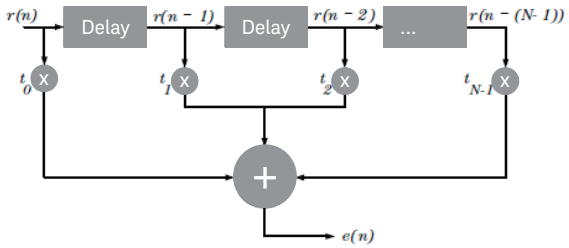
We can add an equalizer at the receive end that mitigates these impairments. An equalizer is simply a filter whose response is the inverse of the channel response.



Add a Feed Forward Equalizer (FFE)

For the ***Feed Forward Equalizer***, we define the nth received sample as r(n), and the Nth tap coefficient as t(N), then the nth output sample e(n) is:

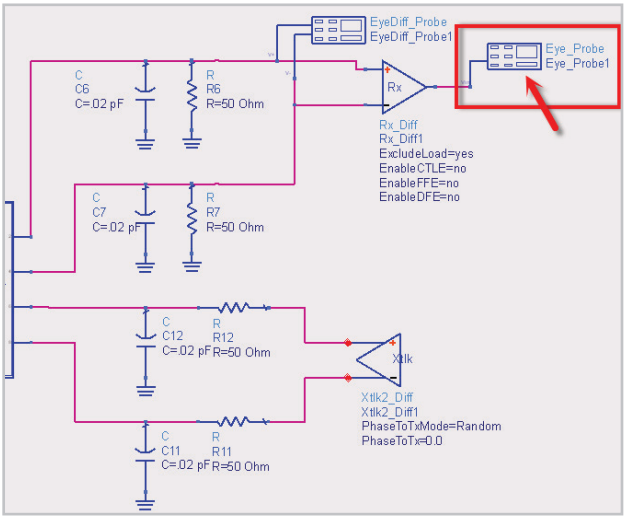
$$e(n) = \sum_{k=0}^{N-1} t(k)\, r(n-k)$$



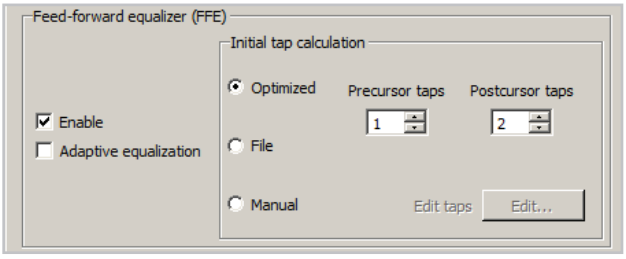
– ***Save*** the 8 Gbps version of the schematic.

– From the ***Simulation-ChanSim palette***, select and place an ***Rx_Diff*** component.

– Add a single-ended eye probe like so:



– Edit ***Rx_Diff1*** and ***Enable the FFE*** with Initial tap calculations as ***Optimized***, number of ***Pre-cursor taps as 1*** and ***Post cursor taps as 2***.



– ***File*** > ***Save Design As***... and enter ***pcie_ffe***.

– ***Simulate***

Equalization Results, Next Steps

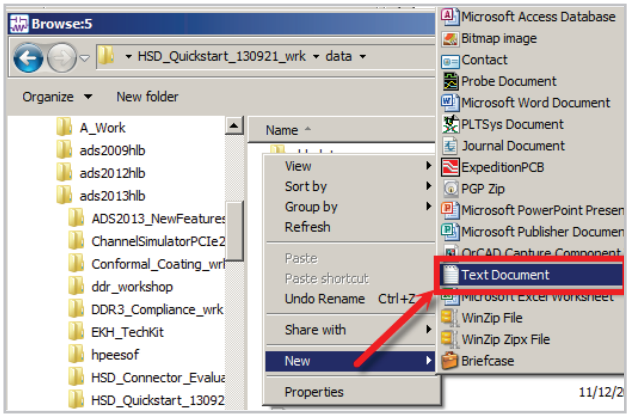
– ***Plot eye diagram*** before equalization and after equalization.

The receiver component has automatically calculated the optimized tap coefficient values. You can output optimized tap coefficients:

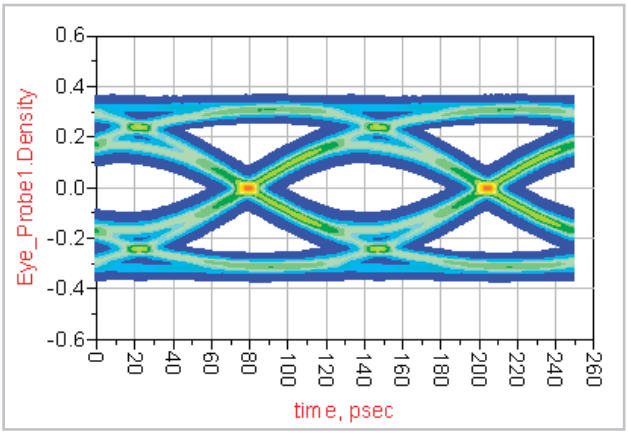
– Double click on ***Rx_Diff1*** and select ***Edit...*** > ***Output*** > ***Browse***.

– In the ***Browse*** window, using right mouse click create a new file ***taps.txt.***

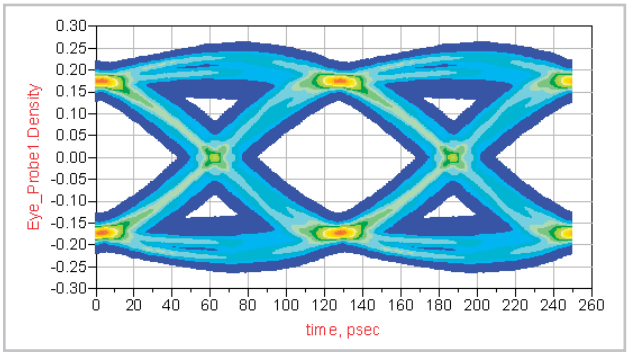
– Re-simulate the design and open ***taps.txt*** file to look at the taps coefficients.



Before FFE



After FFE



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